REMARKS

Claims 1-7, 16-21 and 29-36 are all the claims pending in this application. Applicants amend claims 1, 17, 33 and 34 with features at least supported by FIGS. 4, 6, 7 and 10 of the instant specification.

Claim Rejections - 35 U.S.C. § 112, first paragraph

Claims 1-7, 16-21, 29-36 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. In particular, the Examiner alleges that the newly amended claim language to claims 1, 17, 33 and 34 recites "at least one signal that [sic] '*which controls the switching of the first and second transistors (line 10).*' However, there is no explicit support for this limitation." Further, with regard to claims 2-7, 16, 18-21, 29-32, 35-36, the Examiner contends that these claims are rejected for being dependent upon improperly worded independent claims. Applicants traverse the rejection as follows.

Applicants respectfully submit that FIG. 4 and the corresponding description in paragraphs [37] to [39] of the specification clearly describe a common inversion timing signal line COMD connected to the gates PchTFT41 an NchTFT 42. Furthermore, FIG. 5 shows the relationship between the COMD and VCOM signals. In view of the above, Applicants respectfully submit that it would be apparent to a person of ordinary skill in the art that the specification provides support for the claimed feature of at least one signal line (i.e., COMD) *which controls the switching of the first and second transistors* (PchTFT41 an NchTFT 42).

Claim rejections under 35 U.S.C. § 103(a)

Claims 1, 3, 16-19, 21, 29, 31-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagi et al. (U.S. Patent No.: 7,002,541 B2) in view of Okajima (U.S. Patent No.: 5,793,680).

Claims 5 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagi et al. (U.S. Patent No.: 7,002,541 B2) in view of Okajima (U.S. Patent No.: 5,793,680) and Park et al. (U.S. Patent No.: 7,133,034 B2).

Claims 2, 4, 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagi et al. (U.S. Patent No.: 7,002,541 B2) in view of Okajima (U.S. Patent No.: 5,793,680) and Kubota et al. (U.S. Publication No.: 2002/0075249 Al).

Applicants traverse the rejections for at least the following reasons.

In the Amendment filed August 31, 2009, Applicants submitted that the combination of Yanagi and Okajima fails to teach or suggest "a high level of a signal passing through the at least one signal line is higher than the high level voltage signal supplied by said first voltage supply and a low level of the signal passing through the signal line is lower than the low level voltage signal supplied by said second voltage supply."

In the Response to the Arguments section on page 4 of the Office Action, the Examiner asserts that:

> First of all, the cited portion teaches the claimed limitations but does not provide an explicit advantage as Applicant alleges. Second, even assuming that there is support for the claim

> limitation, that is equally strong support for having the voltage values be *"substantially same"* hence, it would appear that it would be obvious to interchange the two concept, of whether the voltage values are substantially the same or higher/lower than one another, since the device would work equally as well.
>
> Further, the advantages Applicant has cited are not unexpected advantages, and whether the voltages are different -as claimed- or are the same, the end result overall would be equally as efficient in achieving the predictable result of supplying the adequate value to the common.

Applicants respectfully disagree with the Examiner's assertion for at least the following reasons.

In a brief telephone interview conducted on February 18, 2010, Applicants' representative pointed out that pages 22-23 of the Amendment filed August 31, 2009, clearly show how paragraph [41] explicitly describes that the ON resistance of the PchTFT 41 and NchTFT 42 are lowered in view of the specific limitations of claim 1. In response the Examiner suggested that the Applicant resubmit these arguments again for her consideration. Thus, Applicants submit the following.

Applicants respectfully submit that paragraphs 39-41 of the specification describes that:

> The gates of the PchTFT41 and NchTFT 42 are connected to the common inversion timing signal line COMD so as to make the H level of the COMD higher that the VCOMH and L level of the COMD lower that the VCOML.

> FIG. 5 is a timing chart showing operation of the common drive circuit 4 in FIG. 4.
>
> According to this embodiment, a voltage difference between the gate and source of the PchTFT 41 and NchTFT 42 is larger compared to the voltages VCOMH and VCOML so that ON resistances of the PchTFT 41 and NchTFT 42 **can be lowered**.

Accordingly, Applicants' specification does provide, according to an exemplary non-limiting embodiment, at least one advantage (i.e., ON resistances of the PchTFT 41 and NchTFT 42 can be lowered), for the claimed feature discussed above. Since this cited portion of the specification clearly describes that the ON resistances of the transistors 41 and 42 are **lowered** as being one exemplary result of the claimed feature of claim 1, the Examiner's contention that the claimed limitations do not provide an explicit advantage contradicts the disclosure in the specification.

Furthermore, the Examiner asserts that there is "equally strong support for having the voltage values be '*substantially same*' hence, it would appear that it would be obvious to interchange the two concept, of whether the voltage values are substantially the same or higher/lower than one another, since the device would work equally as well." However, the Examiner fails to show support for such an assertion. In particular, the Examiner fails to show support for the assertion that having the voltage values being "substantially same" would result in the ON resistances of the transistors 41 and 42 being **lowered**, which is described as an advantage of the above discussed feature of claim 1.

Also, Applicants submit that claim 1 does not recite the voltage values being substantially the same. Further, Applicants submit that there is no support for the Examiner's assertions that "it would be obvious to interchange the two concept, of whether the voltage values are substantially the same or higher/lower than one another, since the device would work equally as well." Since there is no support for the assertion that having the voltage values being "substantially same" would result in the ON resistances of the transistors 41 and 42 being **lowered**, it would be improper for the Examiner to conclude that the device would work equally as well.

At least for these reasons discussed above, Applicants submit that the voltage values of the signal lines are not an obvious matter of design choice.

In addition, Applicants respectfully submit that Okajima also does not teach or suggest the features of claim 1 missing in Yanagi. For instance, FIG. 14 of Okajima does not teach or suggest that the amplitude of LI and L2 are larger than the level of CLK0 and /CLK0 signals of circuit 61. In column 12, lines 13-15, Okajima discloses that the function of unit 60 is to permit the conversion of high level of CLK into low level and low level of CLK into high level when the control signal FLAG is "on". However, this does not teach or suggest that the amplitude is converted. Therefore, the amplitude of the input signals CLK and /CLK and gate signals L1 and L2 input to the transistors are the same. As such, Okajima does not teach that the amplitude of the gate signals L1 and L2 are higher than that of the input signal CLK and /CLK. Therefore, Okajima does not teach or suggest "a high level of a signal passing through the at least one signal line is higher than the high level voltage signal supplied by said first voltage supply and a low

level of the signal passing through the signal line is lower than the low level voltage signal supplied by said second voltage supply."

Lastly, claim 1 recites, *inter alia*, "at least one capacitance load **directly** connected to respective terminals." Applicants respectfully submit that Yanagi does not teach or suggest this feature of claim 1.

In FIG. 1, Yanagi discloses a display cell 13 connected to switch 5c through a buffer element 4. As such, the display cell 13 (allegedly corresponding to the claimed at least one capacitance load) is **not directly** connected to the switch 5c (allegedly corresponding to the claimed transistors). Therefore, Yanagi does not teach or suggest "at least one capacitance load **directly** connected to respective terminals."

In view of the above, Applicants respectfully submit that claim 1 is patentable over the cited combination of references.

Claims 17, 33 and 34

Applicants respectfully submit that claims 17, 33 and 34 recite subject matter analogous to claim 1, and therefore are allowable for at least analogous reasons claim 1 is allowable.

Claims 3, 16, 18, 19, 21, 29-32, 35 and 36

Applicants submit that claims 2-4, 6, 7, 18, 19, 21, 29-32, 35 and 36 depend from one of the independent claims that have been shown to be allowable, and therefore these claims are allowable at least by virtue of there dependency and the additional features recited therein.

Claims 2, 4, 6 and 7

Applicants submit that since claims 2, 4, 6 and 7 depend from one of the claims that have been shown to be allowable and since Kubota does not teach or suggest the features of claim 1 missing in Yanagi and Okajima, these claims are also allowable at least by virtue of their dependency and the additional features recited therein.

With regard to claim 2, Applicants respectfully submit that the cited combination of the references do not teach or suggest "said common drive circuit is disposed on a position opposite to said gate driver circuit and said display portion therebetween." In FIG. 1 of Yanagi, the buffer element 4 and the offset voltage setting section 5 are not disposed on the **opposite side** of the scanning line driving circuit 2 (allegedly corresponding to the claimed gate driver circuit). On the contrary, the scanning line driving circuit 2 is shown to be above the offset voltage setting section 5.

Claims 5 and 20

Applicants submit that since claims 5 and 20 depend from one of the claims that have been shown to be allowable and since Park does not teach or suggest the features of claim 1 missing in Yanagi and Okajima, these claims are also allowable at least by virtue of their dependency and the additional features recited therein.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the

Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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